**IN THE CLAIMS:**

Please amend claim 1 and add new claims 2-14 as follows:

1. (currently amended) A semiconductor integrated circuit device comprising:

a first ~~control~~ circuit ~~for controlling a well bias of a PMOS~~ comprising a first MOS transistor of a first conductivity type and a second MOS transistor of a second conductivity type, ~~and an NMOS transistor, the control circuit being formed in a part of a region for forming a main circuit constructed mainly by a CMOS formed by the PMOS and NMOS transistors during a process of forming said main circuit,~~

a delay monitor circuit comprising a third MOS transistor of the first conductivity type and a fourth MOS transistor of the second conductivity type, and outputting a delay signal, ~~wherein said control circuit has: means for detecting a deviation of delay time of a critical path having the longest delay time formed in said main circuit from a design parameter and determining said well bias in accordance with the deviation; and means for detecting a difference between a threshold voltage of said PMOS transistor and a threshold voltage of said NMOS transistor, and said control circuit has a function of correcting said well bias in accordance with the difference output.~~

a comparator comparing the delay signal with a clock signal and outputting a first control signal and a second control signal,

a well bias voltage generator outputting a first well bias voltage to the first MOS transistor and the third MOS transistor and outputting a second well bias voltage to the second MOS transistor and the fourth MOS transistor, and

a compensation circuit comprising a fifth MOS transistor of the first conductivity type and a sixth MOS transistor of the second conductivity type, and outputting a difference signal, the difference signal based on the difference between a threshold voltage of the fifth MOS transistor and a threshold voltage of the sixth MOS transistor,

wherein the well bias voltage generator outputs the first well bias voltage controlled by the first control signal and outputs the second well bias voltage controlled by the second control signal adjusted by the difference signal.

2. (new) A semiconductor integrated circuit device according to claim 1,

wherein the compensation circuit further comprises,

a first CMOS inverter comprising the fifth MOS transistor and the sixth MOS transistor and outputting a first logical threshold voltage,

a reference voltage generator outputting a first reference voltage and a second reference voltage lower than the first reference voltage,

a comparator comparing the logical threshold voltage with the first and second reference voltages, and outputting a first signal and a second signal, and

a difference detector detecting the difference between the first signal and the second signal, and outputting the difference signal.

3. (new) A semiconductor integrated circuit device according to claim 2,

wherein the comparator outputs the first signal when the first logical threshold voltage is higher than the first reference voltage, and output the second signal when the first logical threshold voltage is lower than the second reference voltage.

4. (new) A semiconductor integrated circuit device according to claim 1,

wherein the compensation circuit further comprises,

a first CMOS inverter comprising the fifth MOS transistor and the sixth MOS transistor and outputting a first logical threshold voltage,

a comparator comprising a second CMOS inverter having a second logical threshold voltage, and a third CMOS inverter having a third logical threshold voltage lower than the second logical threshold voltage, comparing the first logical threshold voltage with the second and third threshold voltages and outputting a first signal and a second signal,

a difference detector detecting the difference between the first signal and the second signal, and outputting the difference signal.

5. (new) A semiconductor integrated circuit device according to claim 4,

wherein the comparator outputs the first signal when the first logical threshold voltage is higher than the second logical threshold voltage, and outputs the second signal when the first logical threshold voltage is lower than the third logical threshold voltage.

6. (new) A semiconductor integrated circuit device according to claim 1,

wherein the well bias voltage generator changes the second control signal in comparison to the first signal based on the difference signal by using a table lookup method.

7. (new) A semiconductor integrated circuit device according to claim 1,

wherein the first circuit further comprises a critical path comprising the first MOS transistor and the second MOS transistor, and having a delay time,

wherein the delay monitor circuit further comprises a path comprising the third MOS transistor and the fourth MOS transistor and simulating the critical path, and outputting the delay signal by simulating the delay time.

8. (new) An output method for outputting a well bias voltage to a first circuit comprised of a first MOS transistor of a first conductivity type and a second MOS transistor of a second conductivity type, comprising:

outputting a delay signal from a delay monitor circuit comprising a third MOS transistor of a first conductivity type and a fourth MOS transistor of a second conductivity type,

comparing the delay signal with a clock signal by a comparator,

outputting a first control signal and a second control signal from the comparator,

outputting a difference signal from a compensation circuit, the difference signal based on a difference between a threshold voltage of a fifth MOS transistor of a first conductivity type and a sixth MOS transistor of a second conductivity type,

adjusting the second control signal using the difference signal in comparison to the first control signal, and

outputting a first well bias voltage controlled by the first control signal to the first and third MOS transistors, and outputting a second well bias voltage controlled by the second control signal adjusted by the difference signal to the second and fourth MOS transistors.

9. (new) An output method for outputting a well bias voltage according to claim 8, further comprising:

outputting a first logical threshold voltage from a first CMOS inverter, the first CMOS inverter comprising the fifth MOS transistor and the sixth MOS transistor,

outputting a first reference voltage and a second reference voltage lower than the first reference voltage from a reference voltage generator,

comparing the first logical threshold voltage with the first and second reference voltages by a comparator,

outputting a first signal and a second signal from the comparator to a difference detector, and

outputting the difference signal by detecting a difference of the first signal and the second signal in the difference detector.

10. (new) An output method for outputting a well bias voltage according to claim 9, further comprising:

outputting the first signal when the first logical threshold voltage is higher than the first reference voltage, and outputting the second signal when the first logical threshold voltage is lower than the second reference voltage.

11. (new) An output method for outputting a well bias voltage according to claim 8, further comprising:

outputting a first logical threshold voltage from a first CMOS inverter, the first CMOS inverter comprising the fifth MOS transistor and the sixth MOS transistor,

comparing the first logical threshold voltage with a second logical threshold voltage of a second CMOS inverter, and with a third logical threshold voltage of a third CMOS inverter by a comparator,

outputting a first signal and a second signal from the comparator to a difference detector, and

outputting the difference signal by detecting a difference of the first signal and the second signal in the difference detector.

12. (new) An output method for outputting a well bias voltage according to claim 11, further comprising:

outputting the first signal when the first logical threshold voltage is higher than the second threshold voltage, and outputting the second signal when the first logical threshold voltage is lower than the third logical threshold voltage.

13. (new) An output method for outputting a well bias voltage according to claim 8, further comprising:

adjusting the second control signal using the difference signal in comparison to the first control signal by using a table lookup method.

14. (new) An output method for outputting a well bias voltage according to claim 8, further comprising:

simulating a delay time in a critical path comprising the first MOS transistor and the second MOS transistor by a path comprising the third MOS transistor and the fourth MOS transistor, and

outputting the delay signal from the delay monitor signal by simulating the delay time.